Method, according to claim 34, further comprising:

providing an interposer component having resilient

contact structures on opposite surfaces thereof between the support

substrate and the probe card.

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-44. Method, according to claim 34, wherein:
the support substrate is a space transformer.

45. Method, according to claim 34, wherein:
the probe elements are resilient contact structures.

46. Method, according to claim 34, wherein: the probe elements are composite interconnection elements.

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(AMENDED) Method, according to claim wherein: the probe elements are elongate; and further comprising:

joining pre-fabricated tip structures to the tips of the probe elements.

48. Method, according to claim 47, wherein:

prior to joining, the pre-fabricated tip structures are resident on a sacrificial substrate; and

further comprising:
after joining, removing the sacrificial substrate.

4.9. Method, according to claim 34, wherein:

arranging the probe elements in groups on the support substrate, each group of probe elements corresponding to a plurality of die sites on a semiconductor wafer.

orientation of the support substrate is adjusted by:

altering the orientation of the support substrate so that [the tips of] the probe elements make substantially simultaneous contact with a flat metal plate which is gradually urged against [the tips of] the probe elements.

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Method, according to claim 34, further comprising:

providing resilient contact structures between the support substrate and the probe card.

Method, according to claim 34, wherein:

the probe elements are positioned approximately in a first plane having an orientation relative to the support substrate;

the probe card is positioned approximately in a second plane; and

altering the orientation of the support substrate relative to the probe card adjusts the orientation of the first plane of the probe elements relative to the second plane of the probe card.

Method, according to claim 34, wherein:

the semiconductor devices are resident on a semiconductor wafer.

In a probe card assembly, a method of altering the orientation of probe elements for probing semiconductor devices, comprising:

providing a probe card; providing a support substrate with plurality of free-

standing resilient probe elements for probing semiconductor devices;

mounting the support substrate on the probe card; and altering the orientation of the support substrate relative to the probe card.

Method, according to claim 54, further comprising:

providing an interposer component having resilient

contact structures on opposite surfaces thereof between the support

substrate and the probe card.

Method, according to claim 4, further comprising:

providing resilient contact structures between the support substrate and the probe card.

Method, according to claim 54, wherein: the support substrate is a space transformer.

Method, according to claim 54, wherein: the probe elements are elongate; and further comprising:

joining pre-fabricated tip structures to the tips of the probe elements.

Method, according to claim 54, wherein:

arranging the probe elements in groups on the support substrate, each group of probe elements corresponding to a plurality of die sites on a semiconductor wafer.

Method, according to claim 54, wherein:
the semiconductor devices are resident on a semiconductor

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wafer.

In a probe card assembly, a method of altering the orientation of probe elements for probing semiconductor devices, comprising:

providing a probe card;

providing a support substrate with plurality of freestanding composite probe elements for probing semiconductor devices;

mounting the support substrate on the probe card; and altering the orientation of the support substrate relative to the probe card.

Method, according to claim 61, further comprising:

providing an interposer component having resilient

contact structures on opposite surfaces thereof between the support

substrate and the probe card.

Method, according to claim 51, further comprising:

providing resilient contact structures between the support substrate and the probe card.

Method, according to claim 52, wherein: the support substrate is a space transformer.

Method, according to claim 1, wherein: the probe elements are elongate; and further comprising:

joining pre-fabricated tip structures to the tips of the probe elements.

Method, according to claim of, wherein:

arranging the probe elements in groups on the support substrate, each group of probe elements corresponding to a plurality of die sites on a semiconductor wafer.

Method, according to claim 61, wherein: the semiconductor devices are resident on a semiconductor wafer.

In a probe card assembly, a method of altering the orientation of probe elements for probing semiconductor devices, comprising:

providing a probe card;

providing a support substrate with plurality of probe elements for probing semiconductor devices;

mounting the support substrate on the probe card; and altering the orientation of the probe elements relative to the probe card by altering the orientation of the support substrate relative to the probe card.

Method, according to claim 68, wherein: the probe elements are free-standing and resilient.

Method, according to claim 58, wherein: the probe elements are free-standing and composite.

Method, according to claim s, further comprising:

providing an interposer component having resilient

contact structures on opposite surfaces thereof between the support

substrate and the probe card.

Method, according to claim 68 further comprising: providing resilient contact structures between the support substrate and the probe card.

Method, according to claim 60, wherein: the support substrate is a space transformer.

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Method, according to claim wherein: the probe elements are elongate; and

further comprising:

joining pre-fabricated tip structures to the tips of the probe elements.

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Method, according to claim 88, wherein:

arranging the probe elements in groups on the support substrate, each group of probe elements corresponding to a plurality of die sites on a semiconductor wafer.

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Method, according to claim 5, wherein:

the semiconductor devices are resident on a semiconductor

wafer. --